gigaSOM gS01Carrier

HW Manual

September 2019

gigaSOM gS01 Carrier

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Reference		
Cross Reference	Filename	Description
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Document contains		
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	Usability Specs	
	Techical Specs	
	Test Procedures	
	Technical Documentation	
v	User Documentation	

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1 Introduction

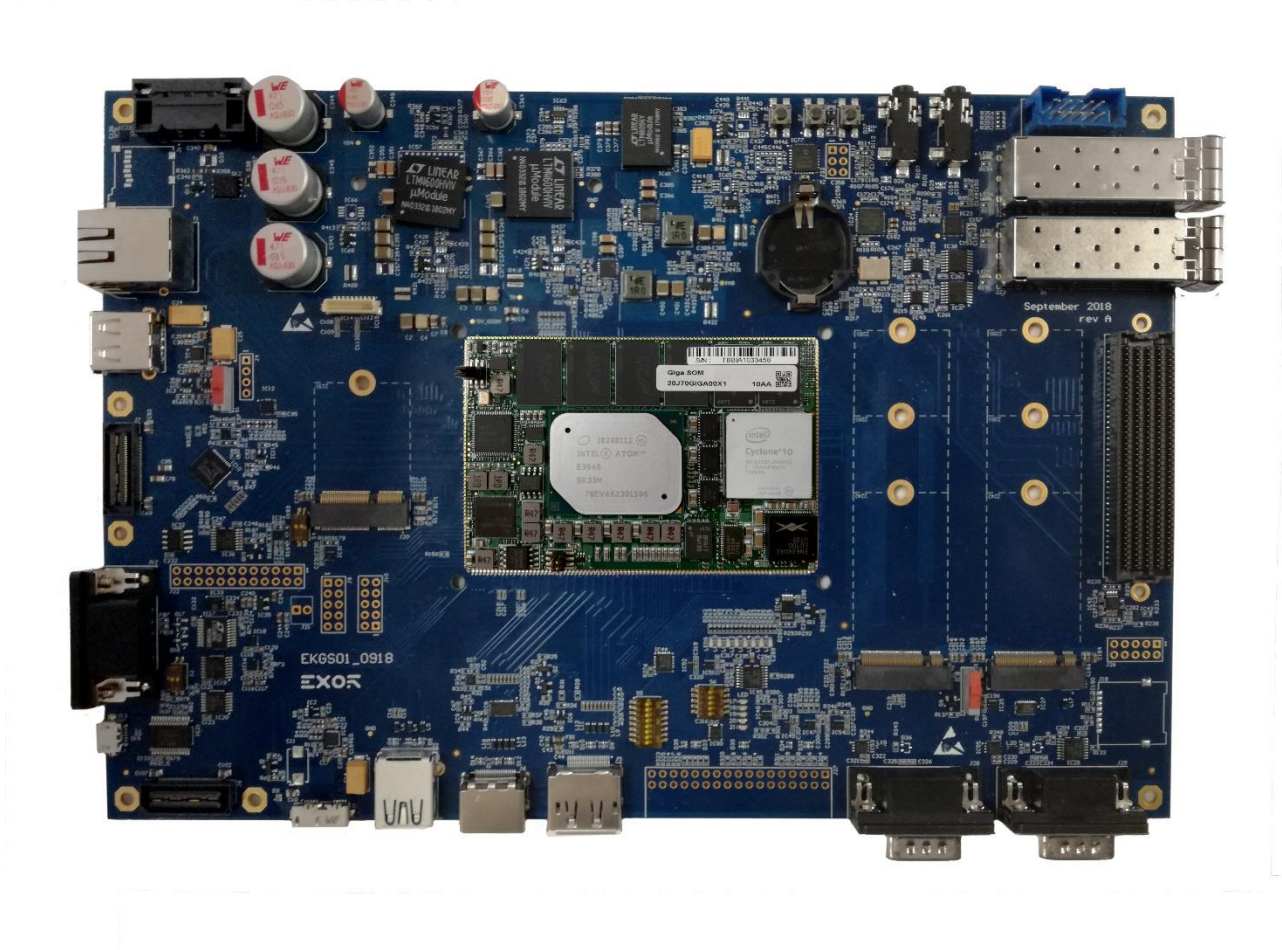

Figure 1. gigaSOM Carrier

The gigaSOM carrier is a flexible development environment with which you can explore and evaluate the functionality and performance of the gigaSOM module which is soldered directly into the gigaSOM Carrier board.

This HW manual describes the gigaSOM carrier board. This document provides information about the features and communication interfaces available on gigaSOM Carrier.

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2 Features

This chapter will show technical and mechanical details of gigaSOM carrier.

2.1 Layout and Communication Interfaces

The photo of the gigaSOM carrier is shown in Figure 2. They depict
the layout of the board and indicates the location of the communication interfaces.

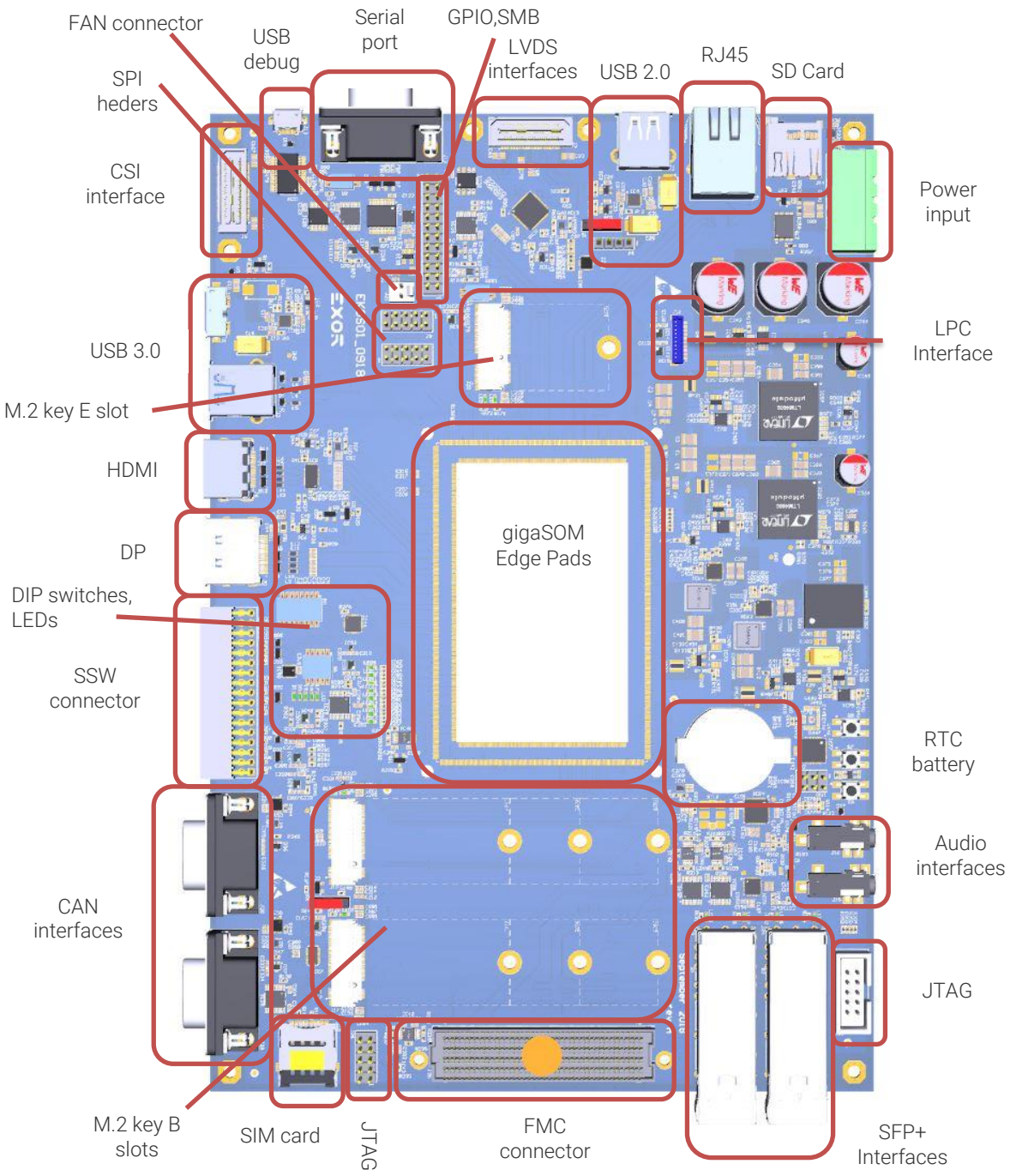

Figure 2. The gigaSOM Carrier and Component Diagram

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The following features and communication interfaces are provided on the gigaSOM carrier:

- 2x USB 2.0 port
- 2x USB 3.0 port
- HDMI Port
- DisplayPort
- RJ45 Ethernet
- Micro SD Card
- 2x Audio Interfaces
- Dual Channel LVDS Interface
- CSI Interface
- Serial Port
- FAN Connector
- 2x M.2 Key B slots
- M.2 Key E slot
- SIM Card
- LPC Interface
- USB Debug Port
- 2x SPI Headers
- GPIO, SMB Header
- EEPROM
- Temperature Sensor
- RTC Battery
- 2x CAN Interfaces
- FMC Connector
- 2x JTAG
- 2x SFP+ Interfaces
- 2x GPIO, DIP Switches Controlled LEDs
- SSW Connector
- 3x Buttons

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2.2 Block Diagram

This section shows the block diagram of gigaSOM carrier. Figure 3.

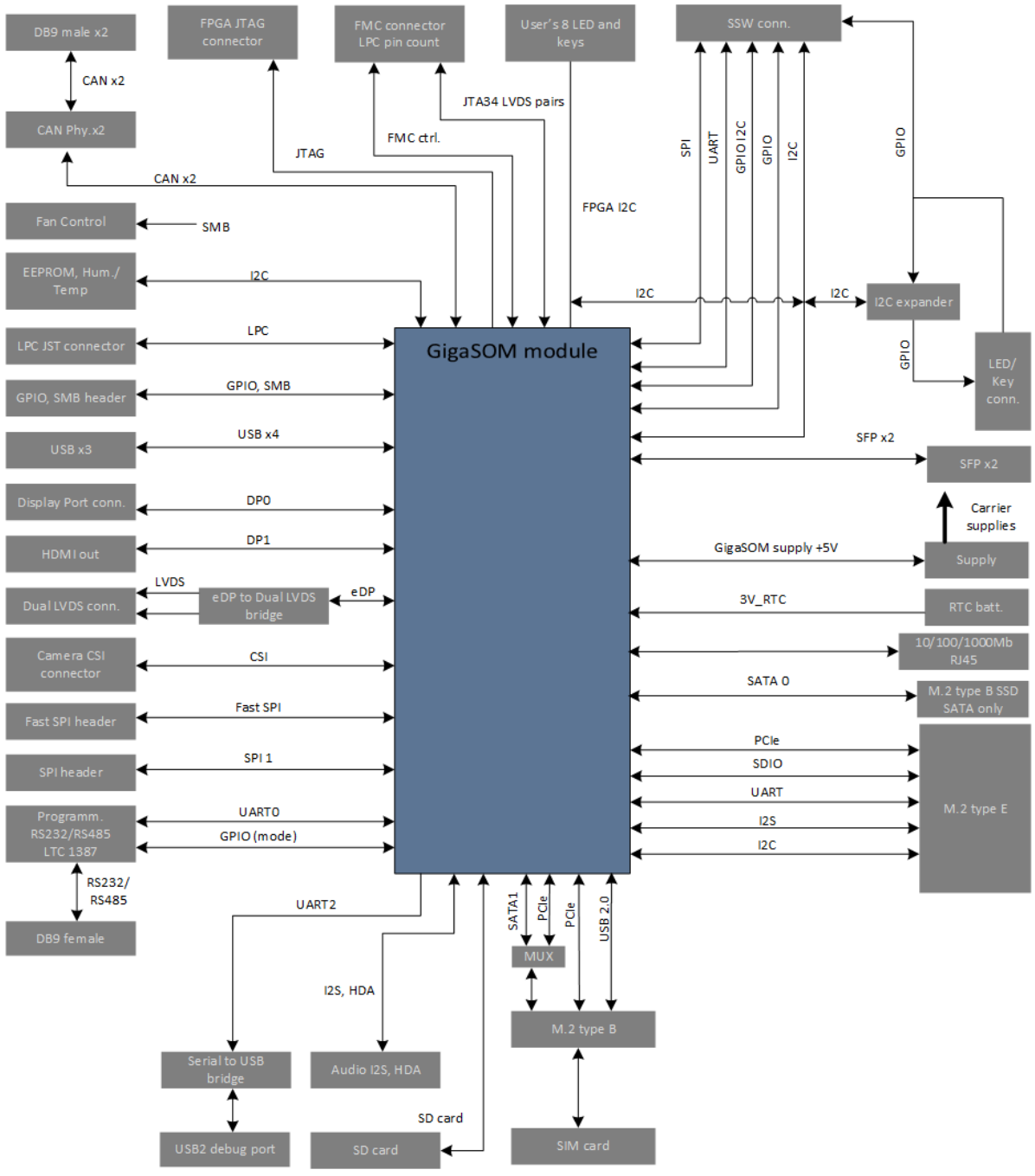

Figure 3. Block Diagram

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2.3 gigaSOM Edge Pads

This section shows the gigaSOM edge pads pinout of gigaSOM module. Table 1.

Pin name	Pin	Connector		Pin name	Pin	Connector
GND	TL1	External left				
SDCARD_D0	TL2	External left				
SDCARD_D1	TL3	External left				
SDCARD_D2	TL4	External left				
SDCARD_D3	TL5	External left				
GND	TL6	External left		LPC_AD0	BL1	Internal left
SDCARD_CMD	TL7	External left		LPC_AD1	BL2	Internal left
SDCARD_CD	TL8	External left		LPC_AD2	BL3	Internal left
SDCARD_WP	TL9	External left		LPC_AD3	BL4	Internal left
SDCARD_CLK	TL10	External left		GND	BL5	Internal left
SDCARD_PWR_EN	TL11	External left		LPC_FRAME	BL6	Internal left
GND	TL12	External left		LPC_SERIRQ	BL7	Internal left
LAN_MDI3N	TL13	External left		LPC_CLKRUN	BL8	Internal left
LAN_MDI3P	TL14	External left		LPC_CLK0	BL9	Internal left
LAN_LINK100#	TL15	External left		GND	BL10	Internal left
LAN_LINK1G#	TL16	External left		USB2_N5	BL11	Internal left
LAN_MDI2N	TL17	External left		USB2_P5	BL12	Internal left
LAN_MDI2P	TL18	External left		GND	BL13	Internal left
LAN_LED_ACT#	TL19	External left		USB2_N4	BL14	Internal left
LAN_MDI1N	TL20	External left		USB2_P4	BL15	Internal left
LAN_MDI1P	TL21	External left		GND	BL16	Internal left

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LAN_GTREF	TL22	External left		USB2_N3	BL17	Internal left
LAN_MDI0N	TL23	External left		USB2_P3	BL18	Internal left
LAN_MDI0P	TL24	External left		GND	BL19	Internal left
GND	TL25	External left		USB2_N2	BL20	Internal left
EDP_HDP	TL26	External left		USB2_P2	BL21	Internal left
EDP_AUXN	TL27	External left		GND	BL22	Internal left
EDP_AUXP	TL28	External left		USB2_N1	BL23	Internal left
GND	TL29	External left		USB2_P1	BL24	Internal left
EDP_TXN0	TL30	External left		GND	BL25	Internal left
EDP_TXP0	TL31	External left		USB2_N0	BL26	Internal left
EDP_TXN1	TL32	External left		USB2_P0	BL27	Internal left
EDP_TXP1	TL33	External left		GND	BL28	Internal left
GND	TL34	External left		USB2_OTG_ID	BL29	Internal left
EDP_TXN2	TL35	External left		USB2_VBUS_SNS	BL30	Internal left
EDP_TXP2	TL36	External left		USB_OC1	BL31	Internal left
EDP_TXN3	TL37	External left		USB_OC0	BL32	Internal left
EDP_TXP3	TL38	External left		GND	BL33	Internal left
GND	TL39	External left		GPIO15	BL34	Internal left
UART2_RTS	TL40	External left		GPIO14	BL35	Internal left
UART2_CTS	TL41	External left		GPIO13	BL36	Internal left
UART2_RXD	TL42	External left		GPIO12	BL37	Internal left
UART2_TXD	TL43	External left		GPIO11	BL38	Internal left
UART1_RTS	TL44	External left		GPIO10	BL39	Internal left
UART1_CTS	TL45	External left		GPIO9	BL40	Internal left

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UART1_RXD	TL46	External left		GPIO7	BL41	Internal left
UART1_TXD	TL47	External left		GPIO6	BL42	Internal left
UART0_RTS	TL48	External left		GPIO5	BL43	Internal left
UART0_CTS	TL49	External left				
UART0_RXD	TL50	External left				
UART0_TXD	TL51	External left				
GND	TL52	External left				
PMU_SUSCLK	TL53	External left				
CB_POK	TL54	External left				
GPIO4	TL55	External left				
GPIO3	TL56	External left				
GPIO2	TL57	External left				
GPIO1	TL58	External left				
F_FMC_LA_TXN10	TR1	External right				
F_FMC_LA_TXP10	TR2	External right				
F_FMC_LA_TXN12	TR3	External right				
F_FMC_LA_TXP12	TR4	External right				
GND	TR5	External right				
F_FMC_LA_TXN9	TR6	External right		F_FMC_LA_RXN13	BR1	Internal right
F_FMC_LA_TXP9	TR7	External right		F_FMC_LA_RXP13	BR2	Internal right
F_FMC_LA_TXN11	TR8	External right		GND	BR3	Internal right
F_FMC_LA_TXP11	TR9	External right		F_FMC_LA_RXN11	BR4	Internal right
GND	TR10	External right		F_FMC_LA_RXP11	BR5	Internal right
F_SPI_CLK_1V5	TR11	External right		F_FMC_LA_RXN15	BR6	Internal right

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F_SPI_CS0_1V5	TR12	External right		F_FMC_LA_RXP15	BR7	Internal right
F_SPI_MISO_1V5	TR13	External right		GND	BR8	Internal right
F_SPI_CS1_1V5	TR14	External right		F_FMC_LA_RXN8	BR9	Internal right
F_SPI_MOSI_1V5	TR15	External right		F_FMC_LA_RXP8	BR10	Internal right
GND	TR16	External right		F_FMC_LA_RXN10	BR11	Internal right
F_CAN_RX2_1V5	TR17	External right		F_FMC_LA_RXP10	BR12	Internal right
F_CAN_TX2_1V5	TR18	External right		GND	BR13	Internal right
F_CAN_RX1_1V5	TR19	External right		F_FMC_DP_C2M_RES_N	BR14	Internal right
F_CAN_TX1_1V5	TR20	External right		F_FMC_DP_C2M_RES_P	BR15	Internal right
F_FMC_SCL	TR21	External right		F_SPF_REFCLK_N	BR16	Internal right
F_FMC_SDA	TR22	External right		F_SPF_REFCLK_P	BR17	Internal right
GND	TR23	External right		GND	BR18	Internal right
F_FMC_DP_M2C_N	TR24	External right		F_SPF_RX1_N	BR19	Internal right
F_FMC_DP_M2C_P	TR25	External right		F_SPF_RX1_P	BR20	Internal right
F_FMC_DP_C2M_N	TR26	External right		F_SPF_TX1_N	BR21	Internal right
F_FMC_DP_C2M_P	TR27	External right		F_SPF_TX1_P	BR22	Internal right
GND	TR28	External right		GND	BR23	Internal right
F_FMC_GBTCLK_M2C_N0	TR29	External right		F_SPF_RX0_N	BR24	Internal right
F_FMC_GBTCLK_M2C_P0	TR30	External right		F_SPF_RX0_P	BR25	Internal right
GND	TR31	External right		F_SPF_TX0_N	BR26	Internal right
F_FMC_LA_TXN8	TR32	External right		F_SPF_TX0_P	BR27	Internal right
F_FMC_LA_TXP8	TR33	External right		GND	BR28	Internal right
F_FMC_LA_TXN15	TR34	External right		F_FMC_LA_RXN12	BR29	Internal right
F_FMC_LA_TXP15	TR35	External right		F_FMC_LA_RXP12	BR30	Internal right

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GND	TR36	External right		F_FMC_LA_RXN9	BR31	Internal right
F_FMC_LA_TXN13	TR37	External right		F_FMC_LA_RXP9	BR32	Internal right
F_FMC_LA_TXP13	TR38	External right		GND	BR33	Internal right
F_FMC_LA_TXN14	TR39	External right		F_FMC_LA_CC_N1	BR34	Internal right
F_FMC_LA_TXP14	TR40	External right		F_FMC_LA_CC_P1	BR35	Internal right
GND	TR41	External right		F_FMC_CLK_M2C_N1	BR36	Internal right
F_FMC_LA_TXN2	TR42	External right		F_FMC_CLK_M2C_P1	BR37	Internal right
F_FMC_LA_TXP2	TR43	External right		GND	BR38	Internal right
F_FMC_LA_TXN1	TR44	External right		F_FMC_CLK_M2C_N0	BR39	Internal right
F_FMC_LA_TXP1	TR45	External right		F_FMC_CLK_M2C_P0	BR40	Internal right
GND	TR46	External right		F_FMC_LA_CC_N0	BR41	Internal right
F_FMC_LA_TXN0	TR47	External right		F_FMC_LA_CC_P0	BR42	Internal right
F_FMC_LA_TXP0	TR48	External right		GND	BR43	Internal right
GND	TR49	External right				
F_FMC_LA_TXN6	TR50	External right				
F_FMC_LA_TXP6	TR51	External right				
F_FMC_LA_TXN5	TR52	External right				
F_FMC_LA_TXP5	TR53	External right				
GND	TR54	External right				
F_FMC_LA_TXN4	TR55	External right				
F_FMC_LA_TXP4	TR56	External right				
F_FMC_LA_TXN3	TR57	External right				
F_FMC_LA_TXP3	TR58	External right				
5VSB	TT1	External top				

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5VSB	TT2	External top				
5VSB	TT3	External top				
5VSB	TT4	External top				
5VSB	TT5	External top				
5VSB	TT6	External top				
5VSB	TT7	External top				
5VSB	TT8	External top				
5VSB	TT9	External top				
5VSB	TT10	External top				
GND	TT11	External top				
GND	TT12	External top				
GND	TT13	External top				
GND	TT14	External top				
GND	TT15	External top				
GND	TT16	External top				
GND	TT17	External top				
GND	TT18	External top				
SDIO_D0	TT19	External top				
SDIO_D1	TT20	External top				
SDIO_D2	TT21	External top				
SDIO_D3	TT22	External top				
SDIO_CMD	TT23	External top				
SDIO_CLK	TT24	External top				
GND	TT25	External top				

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HDA_SPKR	TT26	External top				
HDA_WS_SYNC	TT27	External top				
HDA_SDO	TT28	External top				
HDA_SDI	TT29	External top				
HDA_BCLK	TT30	External top				
HDA_RST_N	TT31	External top				
GND	TT32	External top				
CAM_MCK	TT33	External top				
CAM_I2C2_SCL	TT34	External top				
CAM_I2C2_SDA	TT35	External top				
CAM1_PWR	TT36	External top				
CAM1_RST	TT37	External top				
GND	TT38	External top				
SMB_CLK_3P3	TT39	External top				
SMB_DATA_3P3	TT40	External top				
SMB_ALERT	TT41	External top				
VCCRTC_3P3	TT42	External top				
GND	TT43	External top				
SATA_LED_N	TT44	External top				
LPSS_I2C0_SDA	TT45	External top				
LPSS_I2C0_SCL	TT46	External top				
LPSS_I2C1_SDA	TT47	External top				
LPSS_I2C1_SCL	TT48	External top				
LPSS_I2C2_SDA	TT49	External top				

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LPSS_I2C2_SCL	TT50	External top				
LPSS_I2C3_SDA	TT51	External top				
LPSS_I2C3_SCL	TT52	External top				
GND	TT53	External top				
POWERBTNIN_N	TT54	External top				
PMU_RSTBTN#	TT55	External top				
PLTRST_N	TT56	External top				
SOC_SLP_S3_N	TT57	External top				
1V8A	TT58	External top				
GND	TT59	External top				
AVS_I2S2_SYNC	TT60	External top				
AVS_I2S2_SDO	TT61	External top				
AVS_I2S2_SDI	TT62	External top				
AVS_I2S2_BCLK	TT63	External top				
GND	TT64	External top				
AVS_I2S1_SDI	TT65	External top				
AVS_I2S1_SYNC	TT66	External top				
AVS_I2S1_MCLK	TT67	External top				
AVS_I2S1_SDO	TT68	External top				
AVS_I2S1_BCLK	TT69	External top				
VCC_ADJ_F	TT70	External top				
VCC_ADJ_F	TT71	External top				
VCC_ADJ_F	TT72	External top				
VCC_ADJ_F	TT73	External top				

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F_GPIO_0	TT74	External top				
F_GPIO_1	TT75	External top				
F_GPIO_2	TT76	External top				
F_GPIO_3	TT77	External top				
F_GPIO_4	TT78	External top				
F_EN_GROUP4	TT79	External top				
IO_INT*	TT80	External top				
F_FPGA_TMS	TT81	External top				
F_FPGA_TDI	TT82	External top				
F_FPGA_TDO	TT83	External top				
F_FPGA_TCK	TT84	External top				
GND	TT85	External top				
F_SPF0_SDA	TT86	External top				
F_SPF0_SCL	TT87	External top				
F_FMC_LA_TXN7	TT88	External top				
F_FMC_LA_TXP7	TT89	External top				
SOC_PWM3	TB1	External bottom				
SOC_PWM2	TB2	External bottom				
SOC_PWM1	TB3	External bottom				
SOC_PWM0	TB4	External bottom				
GND	TB5	External bottom				
SATA_RXN1	TB6	External bottom		GPIO8	BB1	Internal bottom
SATA_RXP1	TB7	External bottom		GND	BB2	Internal bottom
SATA_TXN1	TB8	External bottom		SIO_SPI1_FS0	BB3	Internal bottom

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SATA_TXP1	TB9	External bottom		SIO_SPI1_RXD	BB4	Internal bottom
GND	TB10	External bottom		SIO_SPI1_TXD	BB5	Internal bottom
SATA_RXN0	TB11	External bottom		SIO_SPI1_CLK	BB6	Internal bottom
SATA_RXP0	TB12	External bottom		SIO_SPI1_FS1	BB7	Internal bottom
SATA_TXN0	TB13	External bottom		GND	BB8	Internal bottom
SATA_TXP0	TB14	External bottom		FST_SPI_HOLD#	BB9	Internal bottom
GND	TB15	External bottom		FST_SPI_WP#	BB10	Internal bottom
PANEL1_BKLTCTL	TB16	External bottom		FST_SPI_MOSI	BB11	Internal bottom
DDI1_CLK	TB17	External bottom		FST_SPI_MISO	BB12	Internal bottom
DDI1_DATA	TB18	External bottom		FST_SPI_CS2#	BB13	Internal bottom
PANEL1_BKLTEN	TB19	External bottom		FST_SPI_CS1#	BB14	Internal bottom
PANEL1_VDDEN	TB20	External bottom		FST_SPI_CLK	BB15	Internal bottom
DDI1_HPD	TB21	External bottom		GND	BB16	Internal bottom
DDI1_AUXN_R	TB22	External bottom		MCSI_RX_DATA3_N	BB17	Internal bottom
DDI1_AUXP_R	TB23	External bottom		MCSI_RX_DATA3_P	BB18	Internal bottom
GND	TB24	External bottom		MCSI_RX_DATA2_N	BB19	Internal bottom
DDI1_TXN3	TB25	External bottom		MCSI_RX_DATA2_P	BB20	Internal bottom
DDI1_TXP3	TB26	External bottom		GND	BB21	Internal bottom
DDI1_TXN2	TB27	External bottom		MCSI_RX_CLK1_N	BB22	Internal bottom
DDI1_TXP2	TB28	External bottom		MCSI_RX_CLK1_P	BB23	Internal bottom
GND	TB29	External bottom		GND	BB24	Internal bottom
DDI1_TXN1	TB30	External bottom		MCSI_RX_CLK0_N	BB25	Internal bottom
DDI1_TXP1	TB31	External bottom		MCSI_RX_CLK0_P	BB26	Internal bottom
DDI1_TXN0	TB32	External bottom		GND	BB27	Internal bottom

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DDI1_TXP0	TB33	External bottom		MCSI_RX_DATA1_N	BB28	Internal bottom
GND	TB34	External bottom		MCSI_RX_DATA1_P	BB29	Internal bottom
DDI0_TXN3	TB35	External bottom		MCSI_RX_DATA0_N	BB30	Internal bottom
DDI0_TXP3	TB36	External bottom		MCSI_RX_DATA0_P	BB31	Internal bottom
DDI0_TXN2	TB37	External bottom		GND	BB32	Internal bottom
DDI0_TXP2	TB38	External bottom		USB3_RX0N	BB33	Internal bottom
GND	TB39	External bottom		USB3_RX0P	BB34	Internal bottom
DDI0_TXN1	TB40	External bottom		USB3_TX0N	BB35	Internal bottom
DDI0_TXP1	TB41	External bottom		USB3_TX0P	BB36	Internal bottom
DDI0_TXN0	TB42	External bottom		GND	BB37	Internal bottom
DDI0_TXP0	TB43	External bottom		USB3_RX1N	BB38	Internal bottom
GND	TB44	External bottom		USB3_RX1P	BB39	Internal bottom
DDI0_AUXN_R	TB45	External bottom		USB3_TX1N	BB40	Internal bottom
DDI0_AUXP_R	TB46	External bottom		USB3_TX1P	BB41	Internal bottom
DDI0_HPD	TB47	External bottom		GND	BB42	Internal bottom
DDI0_DATA	TB48	External bottom		PCIE2_RESET	BB43	Internal bottom
DDI0_CLK	TB49	External bottom		PCIE_WAKE1#	BB44	Internal bottom
PANEL0_VDDEN	TB50	External bottom		PCIE_CLKREQ2#	BB45	Internal bottom
PANEL0_BKLTEN	TB51	External bottom		GND	BB46	Internal bottom
PANEL0_BKLTCTL	TB52	External bottom		PCIE_CLKOUT2N	BB47	Internal bottom
GND	TB53	External bottom		PCIE_CLKOUT2P	BB48	Internal bottom
PCIE_CLKREQ3#	TB54	External bottom		GND	BB49	Internal bottom
PCIE1_RESET	TB55	External bottom		PCIE_P2_RXN	BB50	Internal bottom
PCIE_WAKE2#	TB56	External bottom		PCIE_P2_RXP	BB51	Internal bottom

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GND	TB57	External bottom		PCIE_P2_TXN	BB52	Internal bottom
PCIE_P0_RXN	TB58	External bottom		PCIE_P2_TXP	BB53	Internal bottom
PCIE_P0_RXP	TB59	External bottom		GND	BB54	Internal bottom
PCIE_P0_TXN	TB60	External bottom		F_FMC_LA_RXN4	BB55	Internal bottom
PCIE_P0_TXP	TB61	External bottom		F_FMC_LA_RXP4	BB56	Internal bottom
GND	TB62	External bottom		GND	BB57	Internal bottom
PCIE_CLKOUT3N	TB63	External bottom		F_FMC_LA_RXN3	BB58	Internal bottom
PCIE_CLKOUT3P	TB64	External bottom		F_FMC_LA_RXP3	BB59	Internal bottom
GND	TB65	External bottom		F_FMC_LA_RXN5	BB60	Internal bottom
PCIE_P1_RXN	TB66	External bottom		F_FMC_LA_RXP5	BB61	Internal bottom
PCIE_P1_RXN	TB67	External bottom		GND	BB62	Internal bottom
PCIE_P1_TXN	TB68	External bottom		F_FMC_LA_RXN6	BB63	Internal bottom
PCIE_P1_TXP	TB69	External bottom		F_FMC_LA_RXP6	BB64	Internal bottom
GND	TB70	External bottom		F_FMC_LA_RXN2	BB65	Internal bottom
F_CTS1_1V5	TB71	External bottom		F_FMC_LA_RXP2	BB66	Internal bottom
F_RTS1_1V5	TB72	External bottom		GND	BB67	Internal bottom
F_RX1_1V5	TB73	External bottom		F_FMC_LA_RXN0	BB68	Internal bottom
F_TX1_1V5	TB74	External bottom		F_FMC_LA_RXP0	BB69	Internal bottom
F_SFP_INT1	TB75	External bottom		F_FMC_LA_RXN1	BB70	Internal bottom
F_SFP_INT0	TB76	External bottom		F_FMC_LA_RXP1	BB71	Internal bottom
F_VREF_FMC	TB77	External bottom				
FMC_PRENT	TB78	External bottom				
GND	TB79	External bottom				
1V5_MEM_F	TB80	External bottom				

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F_SPF1_SCK	TB81	External bottom				
F_SPF1_SDA	TB82	External bottom				
F_SCL	TB83	External bottom				
F_SDA	TB84	External bottom				
GND	TB85	External bottom				
F_FMC_LA_RXN7	TB86	External bottom				
F_FMC_LA_RXP7	TB87	External bottom				
F_FMC_LA_RXN14	TB88	External bottom				
F_FMC_LA_RXP14	TB89	External bottom				

Table 1. gigaSOM Edge Pads

2.4 Temperature Range

Operating Temperature Range
- -40 °C to +85 °C.

2.5 Power Supply

The gigaSOM carrier features the connector 1795679 (J31) for DC power supply.

Pin	Signal name	Description
1	VDD	Input voltage (12 – 24V)
2	GND	Ground
3	SHIELD	Shield

Table 2. Power Connector Description

2.6 RTC Battery

The gigaSOM carrier provides a board-mounted battery holder (BAT1) for a RTC battery. The RTC battery supplies the power required to maintain the module RTC memory. The required battery type on gigaSOM carrier is CR2032

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2.7 FAN Connector

The gigaSOM carrier provides a FAN connector 171856-0002 (J21).

Pin	Signal name	Description
1	+5V_FAN	Output voltage (5V)
2	GND	Ground

Table 3. FAN Connector Description

2.8 Mechanical Dimensions

Figure 4. shows the dimension of gigaSOM carrier.

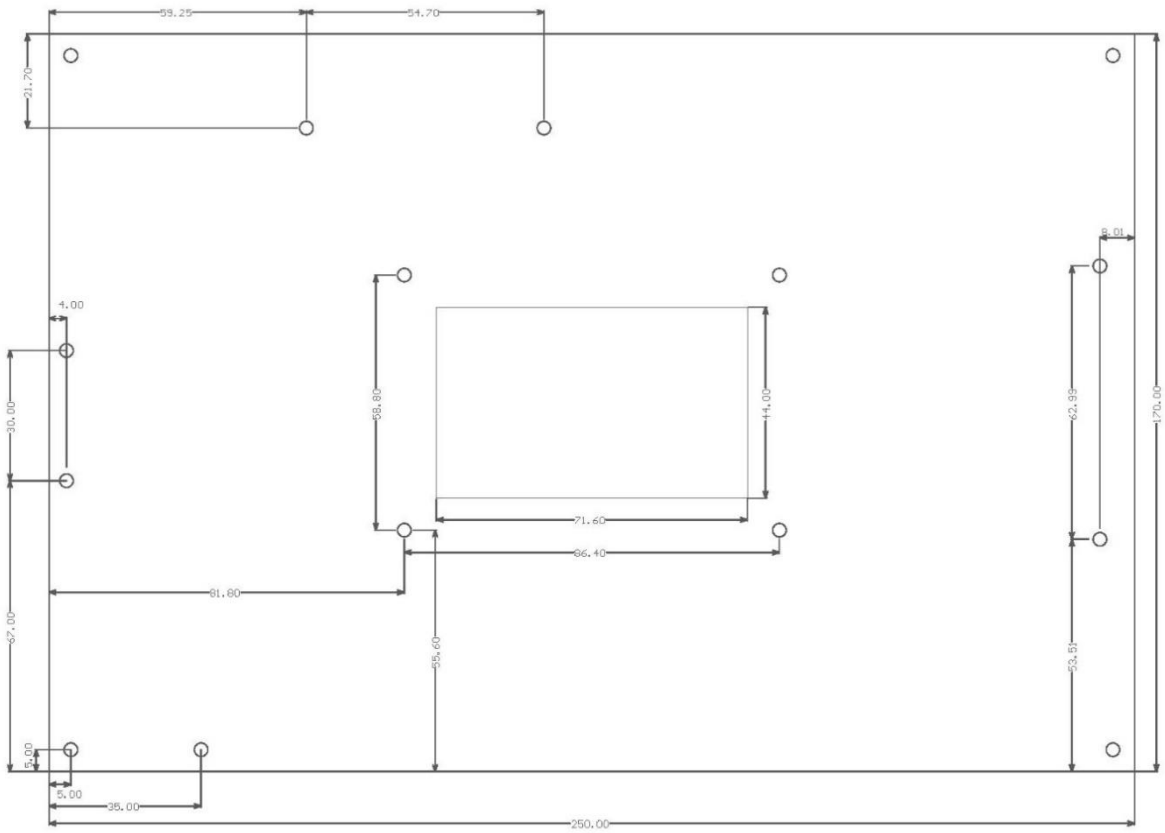

Figure 4. Mechanical Dimensions

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3 Interfaces

This chapter describes the comunication interfaces of gigaSOM carrier.

3.1 USB

The gigaSOM carrier provides the following USB connectors:

3.1.1 Micro USB 3.0 Type B

The gigaSOM carrier features a micro USB 3.0 Type B port with OTG capability (J1) provides up to 900 mA.

3.1.2 USB 3.0 Type A

The gigaSOM carrier features a USB 3.0 Type A port (J2) provides up to 900 mA.

3.1.3 USB 2.0 Type A

The gigaSOM carrier features a USB 2.0 Type A port with (J3) provides up to 450 mA.

3.1.4 USB 2.0 Header

The gigaSOM carrier features a USB 2.0 Header (J4) provides up to 450 mA.

Pin	Signal name	Description
1	+5V_VBUS_4	Output voltage (5V)
2	USB4_D_N	USB Differantial Data Positive
3	USB4_D_P	USB Differential Data Negative
4	GND	Ground

Table 4. USB 2.0 Header Description

USB 2.0 Header is shared with USB 2.0 which is on QTH connector (J7). By using the slide switch (S1), it is possible to determine whether the interface USB 2.0 Header or USB 2.0 QSH.

Slide Switch	Configuration
3	Enable USB 2.0 Header, disable USB 2.0 QSH
2	Enable USB 2.0 QSH, disable USB 2.0 Header

Table 5. Slide Switch S1 Description

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3.1.5 USB 2.0 Debug Port

The gigaSOM carrier features a USB 2.0 Type AB port (J13).

3.2 HDMI

The gigaSOM carrier supports an industry standard HDMI connector type A (J6).

3.3 DisplayPort

The gigaSOM carrier supports a DispalyPort (J5).

3.4 LVDS Interface

For connecting LCD panels and monitors the gigaSOM carrier supports a dual channel LVDS Interface on QSH connector (J7). LVDS signals are converted from eDP over PTN3460I.

Pin	Signal name	Description		Pin	Signal name	Description
1	+12V_CONN	Output voltage (12V)		2	LVDS_A0_N	LVDS Channel A Differantial Data Negative
3	+12V_CONN	Output voltage (12V)		4	LVDS_A0_P	LVDS Channel A Differantial Data Positive
5	+12V_CONN	Output voltage (12V)		6	GND	Ground
7	+12V_CONN	Output voltage (12V)		8	LVDS_A1_N	LVDS Channel A Differantial Data Negative
9	+12V_CONN	Output voltage (12V)		10	LVDS_A1_P	LVDS Channel A Differantial Data Positive
11	SOC_VDD_EN	Panel power enable output		12	GND	Ground
13	SOC_BKLTEN	Backlight enable output		14	LVDS_A2_N	LVDS Channel A Differantial Data Negative
15	SOC_BKLCTL	PWM output signal to display panel		16	LVDS_A2_P	LVDS Channel A Differantial Data Positive
17	GND	Ground		18	GND	Ground
19	+5V	Output voltage (5V)		20	LVDS_ACK_N	LVDS Channel A Differantial ClockNegative
21	+5V	Output voltage (5V)		22	LVDS_ACK_P	LVDS Channel A Differantial Clock Positive
23	+5V	Output voltage (5V)		24	GND	Ground
25	GND	Ground		26	LVDS_A3_N	LVDS Channel A Differantial Data Negative
27	+3V3	Output voltage (3V3)		28	LVDS_A3_P	LVDS Channel A Differantial Data Positive
29	+3V3	Output voltage (3V3)		30	GND	Ground
31	+3V3	Output voltage (3V3)		32	GND	Ground

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33	GND	Ground		34	LVDS_B0_N	LVDS Channel B Differantial Data Negative
35	PVCCEN	Panel power enable output		36	LVDS_B0_P	LVDS Channel B Differantial Data Positive
37	DDC_SDA	DDC data signal		38	GND	Ground
39	DDC_SCL	DDC clock signal		40	LVDS_B1_N	LVDS Channel B Differantial Data Negative
41	PWMO	PWM output signal to display panel		42	LVDS_B1_P	LVDS Channel B Differantial Data Positive
43	BKLTEN	Backlight enable output		44	GND	Ground
45	MS_SDA	I2C-bus data signal		46	LVDS_B2_N	LVDS Channel B Differantial Data Negative
47	MS_SCL	I2C-bus clock signal		48	LVDS_B2_P	LVDS Channel B Differantial Data Positive
49	USB3_PWREN	Power enable for USB 2.0 QSH		50	GND	Ground
51	GND	Ground		52	LVDS_BCK_N	LVDS Channel B Differantial ClockNegative
53	QSH_USB4_D_P	USB Differantial Data Positive		54	LVDS_BCK_P	LVDS Channel B Differantial Clock Positive
55	QSH_USB4_D_N	USB Differential Data Negative		56	GND	Ground
57	GND	Ground		58	LVDS_B3_N	LVDS Channel B Differantial Data Negative
59	+1V8	Output voltage (1V8)		60	LVDS_B3_P	LVDS Channel B Differantial Data Positive
61	GND	Ground		62	GND	Ground
63	GND	Ground		64	GND	Ground

Table 6. LVDS QSH Connector Description

3.5 Gigabit Ethernet

The gigaSOM carrier provides 10/100/1000Base-T Ethernet with magnetic and LEDs (T1).

3.6 Micro SD Card

The gigaSOM carrier features a micro SD card slot (J14).

3.7 Audio Interfaces

The gigaSOM carrier features two audio codecs HDA (CS4207) and I2S (WM8904). Each codecs suport Line-out signals and MIC-in signals on 3.5 mm audio jacks (J15 for I2S codec and J16 for HDA codec).

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3.8 CSI Interface

The gigaSOM carrier provides CSI Interface on QSH connector (J8).

Pin	Signal name	Description	Pin	Signal name	Description
1	+3V3	Output voltage (3V3)	2	SOC_CSI_RX0_P	CSI RX Differantial Data Positive
3	+3V3	Output voltage (3V3)	4	SOC_CSI_RX0_N	CSI RX Differantial Data Negative
5	+3V3	Output voltage (3V3)	6	GND	Ground
7	+3V3	Output voltage (3V3)	8	GND	Ground
9	+3V3	Output voltage (3V3)	10	SOC_CSI_RX1_P	CSI RX Differantial Data Positive
11	+3V3	Output voltage (3V3)	12	SOC_CSI_RX1_N	CSI RX Differantial Data Negative
13	NC	No Connect	14	GND	Ground
15	NC	No Connect	16	GND	Ground
17	NC	No Connect	18	SOC_CSI_CK0_P	CSI Input Differantial Clock Positive
19	NC	No Connect	20	SOC_CSI_CK0_N	CSI Input Differantial Clock Negative
21	NC	No Connect	22	GND	Ground
23	NC	No Connect	24	GND	Ground
25	NC	No Connect	26	NC	No Connect
27	NC	No Connect	28	NC	No Connect
29	NC	No Connect	30	GND	Ground
31	NC	No Connect	32	GND	Ground
33	NC	No Connect	34	SOC_CSI_RX2_P	CSI RX Differantial Data Positive
35	NC	No Connect	36	SOC_CSI_RX2_N	CSI RX Differantial Data Negative
37	NC	No Connect	38	GND	Ground
39	NC	No Connect	40	GND	Ground
41	NC	No Connect	42	SOC_CSI_RX3_P	CSI RX Differantial Data Positive
43	NC	No Connect	44	SOC_CSI_RX3_N	CSI RX Differantial Data Negative
45	1V8A	Output voltage (1V8) from CPU	46	GND	Ground
47	NC	No Connect	48	GND	Ground

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49	GP_CAMERASB06	Camera gpio		50	SOC_CAM_MCK	Camera clock output
51	GP_CAMERASB04	Camera gpio		52	GND	Ground
53	NC	No Connect		54	SOC_I2C_CAM_CLK	I2C-bus clock signal
55	+1V8	Output voltage (1V8)		56	SOC_I2C_CAM_SDA	I2C-bus data signal
57	+1V8	Output voltage (1V8)		58	SOC_CAM_PWRn	Camera gpio
59	+1V8	Output voltage (1V8)		60	SOC_CAM_RSTn	Camera gpio
61	GND	Ground		62	GND	Ground
63	GND	Ground		64	GND	Ground

Table 7. CSI QSH Connector Description

3.9 Serial Port

The gigaSOM carrier support RS232/RS485 serial port on Dsub9 connector (J12). Use DIP Switch (S2) to select RS232 or RS485 interface and select controlled by RTS or CPU.

DIP Switch		Configuration
SW1	SW2	
OFF	OFF	RS485 mode, controlled by RTS
ON	OFF	RS232 mode, controlled by RTS
OFF	ON	RS485 mode, controlled by CPU
ON	ON	RS232 mode, controlled by RTS

Table 8. DIP Switch S2 Description

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3.10 LPC Bus

The gigaSOM carrier features a Low Pin Count bus on JST connector (J11).

Pin	Signal name	Description
1	GND	Ground
2	LPC_CLKRUN	Control LPC Clock Signals
3	LPC_CLK	25 Mhz output clock
4	LPC_FRAME	LFRAME# indicates the start of an LPC cycle, or an abort
5	LPC_AD3	LPC Multiplexed Command, Adddress, Data
6	LPC_AD2	LPC Data
7	LPC_AD1	LPC Data
8	LPC_AD0	LPC Data
9	LPC_SERIRQ	Serial Interrupt Request
10	+3V3	Output voltage (3V3)

Table 9. LPC Bus Description

3.11 SPI Interfaces

The gigaSOM carrier provides SPI signals on header (J9) and Fast SPI Interface on header (J10).

Pin	Signal name	Description		Pin	Signal name	Description
1	+1V8	Output voltage (1V8)		2	+3V3	Output voltage (3V3)
3	SOC_SPI_FS0	Used as the SPI bus request signal		4	SOC_SPI_RXD	Data Input pin for the processor
5	SOC_SPI_TXD	Data Output pin for the processor		6	GND	Ground
7	GND	Ground		8	SOC_SPI_CLK	SPI Clock signal
9	SOC_SPI_FS1	Used as the SPI bus request signal		10	GND	Ground

Table 10. SPI Header Description

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Pin	Signal name	Description		Pin	Signal name	Description
1	+1V8	Output voltage (1V8)		2	+3V3	Output voltage (3V3)
3	SOC_FAST_SPI_CLK	Fast SPI Clock		4	SOC_FAST_SPI_CS1n	Fast SPI Chip Select
5	SOC_FAST_SPI_CS2n	Fast SPI Chip Select		6	SOC_FAST_SPI_MISO	Data Output pin for the SoC
7	SOC_FAST_SPI_MOSI	Data Input pin for the SoC		8	SOC_FAST_SPI_WPn	Write Protect Input
9	SOC_FAST_SPI_HOLDn	Hold or Reset Input		10	GND	Ground

Table 11. Fast SPI Interface Description

3.12 PCIe

The gigaSOM carrier provides three PCIe interfaces: two on M.2 key B slot (J17) and one on M.2 key E slot (J20).

3.12.1 M.2 key B (J17)

The gigaSOM carrier provides an M.2 Key B slot (J17). The M.2 connector (J17) suports multiple interfaces USB 2.0, 2x PCIe, SATA, UIM, I2C.

1x PCIe is shared with SATA. By using the slide switch (S2), it is possible to determine whether the interface PCIe or SATA.

Slide Switch	Configuration
2	Enable PCIe, disable SATA
3	Enable SATA, disable PCIe

Table 12. Slide Switch S2 Description

3.12.1.1 SIM Card

The gigaSOM carrier features a SIM card (J18). The card is connected to the UIM interface of the M.2 connector (J17).

3.12.2 M.2 key E

The gigaSOM carrier provides an M.2 Key E slot (J20) for connecting Wifi, NFC, GNSS and Bluetooth devices. The M.2 connector (J20) suports multiple interfaces USB 2.0, PCIe, SDIO, UART, I2C, I2S.

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3.13 SATA

The gigaSOM carrier provides two SATA interfaces: one on M.2 key B slot (J17) and one on M.2 key B slot (J19).

The M.2 connector (J19) suports SSD Sata only.

3.14 CAN

The gigaSOM carrier provides two CAN interfaces on Dsub9 connectors (J28 and J29).

3.15 SFP+

The gigaSOM carrier provides two SFP+ interfaces (J23 and J24) supporting 10GE. Also carrier features referent clock for SFP generated with Si570 (XTL1). Each SFP+ intreface has two Leds.

LED	Signal name	Description
LED 5	SFP0_RLED	LED is turn ON when SFP0_RLED is DOWN
LED 6	SFP1_RLED	LED is turn ON when SFP1_RLED is DOWN
LED 7	SFP0_GLED	LED is turn ON when SFP0_GLED is DOWN
LED 8	SFP1_GLED	LED is turn ON when SFP1_GLED is DOWN

Table 13. SFP Interface LED Status Description

3.16 FMC

The gigaSOM carrier features a FMC connector (J25). It is a Low Pin Count (LPC) size of connector. The FMC (LPC) Interface on carrier can provides 74 user-define, single-ended signals (include clock signals), 1 serial transceiver pair, I2C and JTAG.

Pin	Bank H	Bank G	Bank D	Bank C
1	+VREF_FMC	GND	FMC_PG_C2M	GND
2	FMC_PRSNT	FMC_CLK0_M2C_P	GND	FMC_DP0_C2M_P
3	GND	FMC_CLK0_M2C_N	GND	FMC_DP0_C2M_N
4	FMC_CLK1_M2C_P	GND	GBTCLK0_M2C_P	GND
5	FMC_CLK1_M2C_N	GND	GBTCLK0_M2C_N	GND
6	GND	FMC_LA_CC0_P	GND	FMC_DP0_M2C_P
7	FMC_LA_TX0_P	FMC_LA_CC0_N	GND	FMC_DP0_M2C_N
8	FMC_LA_TX0_N	GND	FMC_LA_CC1_P	GND

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9	GND	FMC_LA_RX4_P	FMC_LA_CC1_N	GND
10	FMC_LA_RX3_P	FMC_LA_RX4_N	GND	FMC_LA_TX1_P
11	FMC_LA_RX3_N	GND	FMC_LA_TX2_P	FMC_LA_TX1_N
12	GND	FMC_LA_RX5_P	FMC_LA_TX2_N	GND
13	FMC_LA_RX6_P	FMC_LA_RX5_N	GND	GND
14	FMC_LA_RX6_N	GND	FMC_LA_TX9_P	FMC_LA_RX12_P
15	GND	FMC_LA_RX2_P	FMC_LA_TX9_N	FMC_LA_RX12_N
16	FMC_LA_RX0_P	FMC_LA_RX2_N	GND	GND
17	FMC_LA_RX0_N	GND	FMC_LA_RX10_P	GND
18	GND	FMC_LA_RX1_P	FMC_LA_RX10_N	FMC_LA_RX8_P
19	FMC_LA_TX3_P	FMC_LA_RX1_N	GND	FMC_LA_RX8_N
20	FMC_LA_TX3_N	GND	FMC_LA_RX15_P	GND
21	GND	FMC_LA_TX4_P	FMC_LA_RX15_N	GND
22	FMC_LA_TX5_P	FMC_LA_TX4_N	GND	FMC_LA_RX8_P
23	FMC_LA_TX5_N	GND	FMC_LA_TX11_P	FMC_LA_RX8_N
24	GND	FMC_LA_TX6_P	FMC_LA_TX11_N	GND
25	FMC_LA_RX14_P	FMC_LA_TX6_N	GND	GND
26	FMC_LA_RX14_N	GND	FMC_LA_TX9_P	FMC_LA_RX13_P
27	GND	FMC_LA_RX7_P	FMC_LA_TX9_N	FMC_LA_RX13_N
28	FMC_LA_TX14_P	FMC_LA_RX7_N	GND	GND
29	FMC_LA_TX14_N	GND	FMC_TCK	GND
30	GND	FMC_LA_TX13_P	FMC_TDI	FMC_I2C_SCL
31	FMC_LA_TX15_P	FMC_LA_TX13_N	FMC_TDO	FMC_I2C_SDA
32	FMC_LA_TX15_N	GND	+3V3	GND
33	GND	FMC_LA_TX8_P	FMC_TMS	GND
34	FMC_LA_TX12_P	FMC_LA_TX8_N	FMC_TRSTn	FMC_GA0
35	FMC_LA_TX12_N	GND	FMC_GA1	+12V_CONN
36	GND	FMC_LA_TX10_P	+3V3	GND
37	FMC_LA_TX7_P	FMC_LA_TX10_N	GND	+12V_CONN
38	FMC_LA_TX7_N	GND	+3V3	GND

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39	GND	+V_ADJ	GND	+3V3
40	+V_ADJ	GND	+3V3	GND

Table 14. FMC Connector Pinout

3.16.1 FMC JTAG

The gigaSOM carrier features a FMC JTAG on header (J26).

Pin	Signal name	Description		Pin	Signal name	Description
1	FMC_TCK	FMC JTAG Clock		2	GND	Ground
3	FMC_TDO	FMC JTAG Data Out		4	+3V3	Output voltage (3V3)
5	FMC_TMS	FMC JTAG Mode Select		6	NC	No Connect
7	NC	No Connect		8	FMC_TRSTn	FMC JTAG Reset
9	FMC_TDI	FMC JTAG Data In		10	GND	Ground

Table 15. FMC JTAG Pinout

3.17 SSW Connector

The gigaSOM carrier features a SSW Samtec connector (J27). This SSW connector suports multiple interfaces SPI, UART, I2C, two groups of GPIO signals and power supply. On I2C is connected two I/O Expanders, PCA6408A (IC45) and PCAL6416A (IC44). Interfaces on SSW connector are 3V3 tolerant.

Pin	Signal name	Description		Pin	Signal name	Description
1	SPI_CLK	SPI Clock		2	EXT_I2C_SCL	I2C Clock
3	SPI_CS0n	SPI Chip Select 0		4	EXT_12C_SDA	I2C Data
5	SPI_MISO	SPI Master Input Slave Output		6	GND	Ground
7	SPI_CS1n	SPI Chip Select 1		8	EXT_GPIO7	GPIO Signal from I/O Expander
9	SPI_MOSI	SPI Master Output Slave Input		10	EXT_GPIO6	GPIO Signal from I/O Expander
11	GND	Ground		12	EXT_GPIO5	GPIO Signal from I/O Expander
13	UART3_TX	UART Data Output		14	EXT_GPIO4	GPIO Signal from I/O Expander
15	UART3_RX	UART Data Input		16	EXT_GPIO3	GPIO Signal from I/O Expander
17	UART3_RTS	UART Ready to Send		18	EXT_GPIO2	GPIO Signal from I/O Expander

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19	UART3_CTS	UART Clear to Send		20	EXT_GPIO1	GPIO Signal from I/O Expander
21	GND	Ground		22	EXT_GPIO0	GPIO Signal from I/O Expander
23	EXD_FPGA_GPIO_0	GPIO Signal		24	GND	Ground
25	EXD_FPGA_GPIO_2	GPIO Signal		26	EXD_FPGA_GPIO_1	GPIO Signal
27	EXD_FPGA_GPIO_4	GPIO Signal		28	EXD_FPGA_GPIO_3	GPIO Signal
29	+1V8	Output voltage (1V8)		30	+12V_CONN	Output voltage (12V)
31	+3V3	Output voltage (3V3)		32	+5V	Output voltage (5V)
33	+3V3	Output voltage (3V3)		34	+5V	Output voltage (5V)

Table 16. SSW Connector Description

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4 Additional Features

This chapter will show additional features of gigaSOM Carrier.

4.1 Buttons

The gigaSOM carrier features three different buttons. These are two power gigaSOm module reset and system reset .

4.1.1 Power

The gigaSOM module will perform a power reset when this button (S7) is pressed. Button (S9) is reserved and it is not used.

4.1.2 Reset

The gigaSOM module will perform a hard reset when this button (S8) is pressed.

4.2 GPIO, SMB, I2C, PWM Header

The gigaSOM carrier provides GPIO signals generated from I/O Expander (PCA6408A), GPIO and PWM signals from SoC, System Management Bus, I2C Interface. On I2C is connected a 2-Kbit serial EEPROM (M24C02-A125), I/O Expander (PCA6408A) and Digital Relative Humidity sensor with Temperature output (HTU21D(F)).

Pin	Signal name	Description		Pin	Signal name	Description
1	+3V3	Output voltage (3V3)		2	SOC_PMU_PLTRSTn	Platform Reset (3V3)
3	SOC_SMB_ALERTn	SMBus Alert (3V3)		4	+1V8	Output voltage (1V8)
5	SOC_SMB_DATA	SMBus Data (3V3)		6	SOC_GPIO3	GPIO Signal from SoC (1V8)
7	SOC_SMB_DATA	SMBus Clock (3V3)		8	SOC_GPIO4	GPIO Signal from SoC (1V8)
9	EXT_CPU_GPIO4	GPIO Signal from I/O Expander (3V3)		10	SOC_PWM3	PWM Signal (1V8)
11	EXT_CPU_GPIO5	GPIO Signal from I/O Expander (3V3)		12	SOC_PWM2	PWM Signal (1V8)
13	EXT_CPU_GPIO6	GPIO Signal from I/O Expander (3V3)		14	SOC_PWM1	PWM Signal (1V8)
15	EXT_CPU_GPIO7	GPIO Signal from I/O Expander (3V3)		16	SOC_PWM0	PWM Signal (1V8)
17	EXT_CPU_GPIO3	GPIO Signal from I/O Expander (3V3)		18	GND	Ground
19	EXT_CPU_GPIO2	GPIO Signal from I/O Expander (3V3)		20	I2C3_SDA_3V3	I2C Data (3V3)
21	EXT_CPU_GPIO1	GPIO Signal from I/O Expander (3V3)		22	I2C3_SCL_3V3	I2C Clock (3V3)

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23	EXT_CPU_GPIO0	GPIO Signal from I/O Expander (3V3)		24	GND	Ground

Table 17. GPIO, SMB, I2C, PWM Header Description

4.3 LEDs, DIP Switches

The gigaSOM carrier features two groups of LEDs. First group of LEDS controlled by gigaSOM module or manually (DIP switch, S6).

LED	Signal name	Description
LED 17	EXD_FPGA_GPIO_0	LED is turn ON when GPIO_0 is DOWN
LED 18	EXD_FPGA_GPIO_1	LED is turn ON when GPIO_1 is DOWN
LED 19	EXD_FPGA_GPIO_2	LED is turn ON when GPIO_2 is DOWN
LED 20	EXD_FPGA_GPIO_3	LED is turn ON when GPIO_3 is DOWN
LED 21	EXD_FPGA_GPIO_4	LED is turn ON when GPIO_4 is DOWN

Table 18. LED Status (0-4) Description

DIP Switch, S6	Signal name	Description
SW1	EXD_FPGA_GPIO_0	GPIO_0 is DOWN when SW1 is turn ON
SW2	EXD_FPGA_GPIO_1	GPIO_1 is DOWN when SW2 is turn ON
SW3	EXD_FPGA_GPIO_2	GPIO_2 is DOWN when SW3 is turn ON
SW4	EXD_FPGA_GPIO_3	GPIO_3 is DOWN when SW4 is turn ON
SW5	EXD_FPGA_GPIO_4	GPIO_4 is DOWN when SW5 is turn ON

Table 19. DIP Switch (S6) Configuration

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The second group controlled by I/O Expander PCAL6416A (IC44). Also, the gigaSOM carrier features an additional DIP switch (S5) for control GPIOs from I/O Expander.

LED	Signal name	Description
LED9	GPO_0	LED is turn ON when GPO_0 is DOWN
LED10	GPO_1	LED is turn ON when GPO_1 is DOWN
LED11	GPO_2	LED is turn ON when GPO_2 is DOWN
LED12	GPO_3	LED is turn ON when GPO_3 is DOWN
LED13	GPO_4	LED is turn ON when GPO_4 is DOWN
LED14	GPO_5	LED is turn ON when GPO_5 is DOWN
LED15	GPO_6	LED is turn ON when GPO_6 is DOWN
LED16	GPO_7	LED is turn ON when GPO_7 is DOWN

Table 20. LED Status (0-7) Description

DIP Switch, S5	Signal name	Description
SW1	GPI_0	GPI_0 is DOWN when SW1 is turn ON
SW2	GPI_1	GPI_1 is DOWN when SW2 is turn ON
SW3	GPI_2	GPI_2 is DOWN when SW3 is turn ON
SW4	GPI_3	GPI_3 is DOWN when SW4 is turn ON
SW5	GPI_4	GPI_4 is DOWN when SW5 is turn ON
SW6	GPI_5	GPI_5 is DOWN when SW6 is turn ON
SW7	GPI_6	GPI_6 is DOWN when SW7 is turn ON
SW8	GPI_7	GPI_7 is DOWN when SW8 is turn ON

Table 21. DIP Switch (S5) Configuration

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4.4 JTAG

The gigaSOM carrier provides a JTAG interface (J30). This interface is used for programming and debugging gigaSOM module.

Pin	Signal name	Description		Pin	Signal name	Description
1	FMC_TCK	JTAG Clock		2	GND	Ground
3	FMC_TDO	JTAG Data Out		4	+1V8	Output voltage (1V8)
5	FMC_TMS	JTAG Mode Select		6	NC	No Connect
7	NC	No Connect		8	NC	No Connect
9	FMC_TDI	JTAG Data In		10	GND	Ground

Table 22. JTAG Pinout

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